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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,672	03/09/2004	Young-pil Kim	5649-1276	3015

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EXAMINER	
LANDAU, MATTHEW C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,672	KIM ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *8 and 10-40* is/are withdrawn from consideration.

5)☒ Claim(s) *1-7,9,41 and 42* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, Species I in the reply filed on January 9, 2006 is acknowledged.

Claims 8 and 10-40 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention/species, there being no allowable generic or linking claim.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the semiconductor substrate further including a plurality of dynamic random access memory devices thereon (claim 42) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 4 is objected to because of the following informalities: there is insufficient antecedent basis for "the first self-aligned contact pads". Claim 1 defines just one first self-aligned contact pad. It is suggested the claimed be changed to depend from claim 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 9, and 41 are rejected under 35 U.S.C. 102(b) as anticipated by Ikeda et al. (US PGPub 2002/0060332, hereinafter Ikeda) or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ikeda in view of Kato et al. (US Pat. 5,625,591, hereinafter Kato).

Regarding claim 1, Figures 1-4 of Ikeda disclose a word line 9(WL) on a semiconductor substrate; an active region comprising a first impurity doped region 20 and a second impurity

doped region 20; a first self-aligned contact pad 27 electrically connected to the first impurity doped region; a first bit line DL electrically connected to the first self-aligned contact pad; a first probing pad electrically connected to the first bit line; a second self-aligned contact pad 28 electrically connected to the second impurity doped region; a second conductive line SL electrically connected to the second self-aligned contact pad; and a second probing pad electrically connected to the second conductive line. It is considered to be inherent that the first bit line and the second conductive line (common source line shown in Figure 1) are each electrically connected to some type of pad (contact pad, bonding pad, etc.) at some point. The limitation "probing" pad is merely a recitation of intended use that does not structurally distinguish the claimed invention over the prior art. Any pad is capable of being used as a probing pad, if not in the final product than in some intermediate fabrication step. However, if for some reason Applicant can overcome the inherency argument, it would still have been obvious to include a first probing pad connected to the bit line and a second probing pad connected to the second conductive line (source line). Figure 24 of Kato discloses a memory array 112 wherein a first pad 104 is electrically connected to the bit lines BL (when the intervening transistors are "on"0 and a second pad 202 electrically connected to the source lines (not labeled). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Ikeda by including probing pads as taught by Kato for the purpose of testing the threshold voltage of the transistors in the memory array (see col. 19, lines 54-59 and col. 20, lines 38-42 of Kato). Once again, note that the limitation "probing" pad is merely a recitation of intended use that does not structurally distinguish the claimed invention over the prior art.

Regarding claim 2, Figures 1 and 4 of Ikeda discloses both the bit line DL is directly connected to the first self-aligned contact and the second conductive line is connected to the second self-aligned contact. These points of contact can be considered the claimed first and second contacts.

Regarding claim 3, Figures 2 and 4 of Ikeda disclose the first self-aligned contact pad 27 is one of a plurality of discrete first self-aligned contact pads disposed between the word line 9(WL) and a second word line 9(WL).

Regarding claim 4, it is inherent that there is some type of insulating pattern between the first self-aligned contact pads.

Regarding claims 5 and 6, it is inherent that there is some type of metal contact between the bit line and the first probing pad and between the second conductive line (source line) and the second probing pad.

Regarding claim 7, Figures 2 and 4 of Ikeda disclose the second impurity doped region 20 is one of a plurality of second doped impurity regions disposed between the word line 9(WL) and a second word line 9(WL), and wherein the second self-aligned contact pad extends in a continuous line between the word line and the second word line to electrically connect to the plurality of second impurity doped regions.

Regarding claim 9, Figure 1 of Ikeda discloses the second conductive line (common source line shown) is perpendicular to the word line.

Regarding claim 41, Figures 1-4 of Ikeda disclose a semiconductor substrate 1/4 including a plurality of active regions separated by isolation regions 2; a plurality of parallel word lines 9(WL) on the semiconductor substrate with each word line crossing a plurality of the

active regions; an array of transistors (transistors shown in Figure 4, a 1 x 6 array) on the semiconductor substrate, wherein each transistor of the array includes first and second source/drain regions 20 on opposite sides of a respective one of the plurality of word lines, wherein each word line separates the first and second source/drain regions of a plurality of the transistors of the array, and wherein each active region includes two transistors of the array sharing a common source/drain region; a first bit line DL electrically connected to a first source/drain region of each transistor of the array; and a second conductive line (common source line shown in Figure 1) electrically connected to a second source/drain region of each transistor of the array.

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Momohara (US Pat. 6,055,655).

Regarding claim 42, the difference between Ikeda and the claimed invention is the semiconductor substrate further includes a plurality of dynamic random access memory (DRAM) devices thereon. Ikeda only discloses a flash memory device on the substrate (paragraph [0091]). Figures 1A-1C of Momohara discloses a substrate 10 that contains both flash memory devices and DRAM devices. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Ikeda by also including DRAM devices on the same substrate for the purpose of providing an integrated circuit with random access capabilities, while increasing the integration density.

Claims 1 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato in view of Ikeda.

Regarding claim 1, Figure 24 of Kato discloses a word line WL(1) on a semiconductor substrate (not specifically shown but inherently present); an active region comprising a first impurity doped region and a second impurity doped region (inherent for the transistors MC); a first contact pad (inherent) electrically connected to the first impurity doped region; a first bit line BL electrically connected to the first contact pad; a first probing pad 104 electrically connected to the first bit line (when the intervening transistors (111 and 101) are "on"); a second contact pad electrically connected to the second impurity doped region; a second conductive line (not labeled) electrically connected to the second contact pad; a second probing pad 202 electrically connected to the second conductive line (when the intervening transistors are "on"). Note that the limitation "probing" pad is merely a recitation of intended use that does not structurally distinguish the claimed invention over the prior art. Kato does not specifically disclose the contact pads are "self-aligned". Figure 4 of Ikeda discloses bit lines and source lines connected to the respective drain and source impurity regions through self-aligned contacts. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kato by using the self-aligned contacts taught by Ikeda for the purpose of selecting a well-known contact method that can be accomplished through a simply fabrication process.

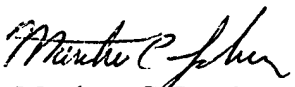
Regarding claim 9, Figure 24 of Kato discloses the second conductive line is perpendicular to the word line WL.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Matthew C. Landau

July 28, 2006